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EXAMINER	
SHRADER, LAWRENCE J	

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/775,119	CLEGG ET AL.
	Examiner	Art Unit
	Lawrence Shrader	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 June 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Applicant's amendment filed on 6/25/2004.

2. The Applicant's arguments have been fully considered, but were not persuasive.

3. Claims 1 – 24 remain rejected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 14, 17, 18; and 19 – 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Benkeser et al., U.S. Patent 5,361,362 (hereinafter referred to as Benkeser).

In regard to claim 14:

"An apparatus for recording segment execution times in a processing system, the apparatus comprising a memory controller in communication with a central processing unit and a memory, the memory controller comprising:

at least one control register;"

See Benkeser column 5, line 47 – 48.

"at least one address register; and"

See Benkeser column 5, line 38 – 40.

"a timestamp assist logic module configured to conduct timestamp update operstions autonomously from the central processing unit by automatically updating a memory location specified by a value in the address register without interaction with the central processing unit."

See Benkeser column 5, line 36 – 48; also Figure 1.

In regard to claim 17, incorporating the rejection of claim 14:

"a processor bus in communication with the central processing unit and the memory controller for communication therebetween;"

See Benkeser Figure 1, ref 131.

"a memory bus in communication with the memory and the memory controller for communication between the memory controller and a plurality of memory locations in the memory;"

See Benkeser Figure 1, ref 131.

"a system bus in communication with the memory controller, the system bus being configured to connect one or more additional devices to the memory controller."

See Benkeser Figure 1, ref 121.

In regard to claim 18, incorporating the rejection of claim 14:

"...wherein the control register is configured to generate an interrupt signal when the timestamp assist module receives a second segment for processing while a first segment is currently processing, the interrupt signal being transmitted to the central processing unit via a system bus."

See Benkeser Figure 1, ref 118 for the interrupt source. Also related text at column 6, lines 1 – 22.

In regard to claim 19 (a memory controller), it is rejected for the same corresponding reasons put forth in the rejection of claim 14 (a corresponding apparatus claim).

In regard to claim 20 (a memory controller) incorporating the rejection of claim 19, it is rejected for the same corresponding reasons put forth in the rejection of claim 15 (a corresponding apparatus claim).

In regard to claim 21, incorporating the rejection of claim 20:

> *"...wherein the elapsed time module comprises a device for calculating and storing an elapsed time value corresponding to the time elapsed between initial segment execution and completion of segment execution."*
>
> See Benkeser Figure 1, ref 115 and 118 and text at column 6, lines 17 – 44.

In regard to claim 22 (a memory controller) incorporating the rejection of claim 20, it is rejected for the same corresponding reasons put forth in the rejection of claim 16 (a corresponding apparatus claim).

In regard to claim 23 (a memory controller) incorporating the rejection of claim 19, it is rejected for the same corresponding reasons put forth in the rejection of claim 17 (a corresponding apparatus claim).

In regard to claim 24, incorporating the rejection of claim 19:

> *"...wherein the timestamp control module is configured to generate an interrupt signal when the timestamp assist logic module receives a second segment for processing while a first segment is currently processing, the interrupt signal being transmitted to a central processing, unit."*
>
> See Benkeser Figure 1, ref 115 and 118 and text at column 6, lines 17 – 44 for the scheduling of segments by using interrupts.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benkeser et al., U.S. Patent 5,361,362 in view of Hurvig et al., U.S. Patent 6,507,592 (hereinafter referred to as Hurvig).

In regard to claim 1:

"A method for recording segment execution times in a processing system, the method comprising the steps of:

> *writing a location for storing a timestamp corresponding, to the beginning of a segment to be executed, the recording step being conducted through a firmware operation; and"*

Benkeser discloses recording time spent in execution of a segment (a timestamp) corresponding to the beginning of a segment to be executed (Abstract; column 2, lines 30 – 46). Although Benkeser does not explicitly disclose a firmware operation, Hurvig discloses recording timestamp operation in firmware (column 19, lines 31 – 34). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the teaching of Benkeser regarding the recording of a timestamp corresponding to the beginning of a segment, with the teaching of Hurvig wherein the timestamp operation is accomplished in firmware, because the use of firmware reduces the interrupt latency as taught by Hurvig (column 19, lines 34 – 35)

"updating the location for storing the timestamp with an elapsed segment execution time, the updating step being conducted through a plurality of hardware based operations autonomously, without firmware interaction."

Benkeser discloses recording a timestamp corresponding to the time spent in executing a segment is recorded (i.e., elapsed time; see column 2, lines 35 – 38). Benkeser does not disclose any firmware interaction, and the underlying processing system is hardware based, including a timer circuit for computing holding time values (column 3, lines 46 – 60; e.g., Figure 1).

In regard to claim 2, incorporating the rejection of claim 1:

"... wherein the recording step comprises writing a first memory address into a globally accessible timestamp address register."

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed (column 2, lines 30 – 46) and the associated process address (see Figure 3). Column 4, lines 1 – 14 describe the master process queue as illustrated in Figure 2. The processes are interpreted as being globally accessible to find the user process storage area.

In regard to claim 6, incorporating the rejection of claim 1:

"...further comprising the step of invoking an interrupt handler if a second segment is received for processing during the updating step."

Benkeser discloses that segment execution is interrupted by a time-slicing scheme to execute segments of several processes (column 5, line 62 to column 6, line 44).

In regard to claim 7, incorporating the rejection of claim 6:

"...wherein the step of invoking an interrupt handler further comprises:
generating an interrupt signal in a memory controller;
determining if the updating step is still in process;
determining if a timeout has been reached if the updating step is determined to still be in process;
restarting the updating step for the second segment; and
clearing the interrupt signal from the memory controller."

Benkeser discloses a segment execution that is interrupted by a time-slice algorithm to execute processes (column 6, lines 17 – 44). The step of generating and clearing an interrupt is inherent in a time-slice algorithm. Benkeser discloses that if a process is partially executed (elapsed time still in process, restarted with each time-slice), a cumulative holding time is computed when the segment is fully executed after the time-slice interrupts.

8. Claims 3, 4; and 8 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benkeser et al., U.S. Patent 5,361,362 in view of Hurvig et al., U.S. Patent 6,507,592, and further in view of Matsuzaki et al., U.S. Patent 6,253,305 (hereinafter referred to as Matsuzaki).

In regard to claim 3, incorporating the rejection of claim 1:

> *"reading the contents of a second memory location designated by an update address register;*
> *"writing the contents of the second memory location into a location value register;*
> *"adding the elapsed segment execution time to the location value register contents;*
> *"storing the location value register contents to the second memory location indicated by the update address register."*

Benkeser discloses recording a timestamp (cumulative hold time) corresponding to the beginning of a segment to be executed, but neither Benkeser nor Hurvig explicitly discloses the addition of elapsed time to a location value register. However, Matsuzaki discloses the steps of reading the contents of a memory designated by an address, writing the contents to a register having another value added to it, and then storing to a location indicated by an address (column 2, lines 5 – 19; e.g., Figures 2A, and 2B). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Benkeser and Hurvig combination of recording of timestamp information in firmware with the addition routine taught by Matsuzaki,

because the combination provides a mechanism to add elapsed timestamp information in the Benkeser invention via the indirect location register.

In regard to claim 4, incorporating the rejection of claim 3:

> *"clearing the elapsed segment execution time stored in an elapsed time register; and*
>
> *"setting a second value in the update address register with a first value from a timestamp address register."*

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed. This process is repeated each time a segment of a process is executed (column 2, lines 35 – 38), which would inherently clear the recorded elapsed segment time with the new time.

In regard to claim 8:

A method for recording segment execution times through a central processing unit, the method comprising the steps of:

> *"writing a first determined memory address into a timestamp address register with a firmware based operation;"*

Benkeser discloses recording time spent in execution of a segment (a timestamp) corresponding to the beginning of a segment to be executed (Abstract; column 2, lines 30 – 46). Although Benkeser does not explicitly disclose a firmware operation, Hurvig discloses recording timestamp operation in firmware (column 19, lines 31 – 34). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the teaching of Benkeser regarding the recording of a timestamp corresponding to the beginning of a segment, with the teaching of Hurvig wherein the timestamp operation is accomplished in firmware,

because the use of firmware reduces the interrupt latency as taught by Hurvig (column 19, lines 34 – 35)

> *"reading contents of the first determined memory address into a location value register with a hardware based operation;*
> *"adding an elapsed time value corresponding to a segment execution time to the contents read into the location value register to create an updated value, the adding step being conducted with a hardware based operation; and*
> *"storing the updated value to the first determined memory address with a hardware based operation."*

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed, but neither Benkeser nor Hurvig explicitly discloses the addition of elapsed time to a location value register. However, Matsuzaki discloses a hardware based operation wherein the steps of reading the contents of a memory designated by an address, writing the contents to a register having another value added to it, and then storing to a location indicated by an address (column 2, lines 5 – 19; e.g., Figures 2A, and 2B). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further combine the recording of timestamp information in firmware as taught by the Benkeser/Hurvig combination with the addition routine taught by Matsuzaki, because the combination provides a mechanism to add elapsed timestamp information in the Benkeser invention via the indirect location register.

In regard to claim 9, incorporating the rejection of claim 8:

> *"reading a memory location from an update address register in a timestamp assist logic module;*
> *"writing the memory location into the location value register in the timestamp assist logic module."*

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed, but neither Benkeser nor Hurvig explicitly reading and writing a memory location from/into an update register. However, Matsuzaki discloses a hardware based operation wherein

the steps of reading the contents of a memory designated by an address, writing the contents to a register having another value added to it, and then storing to a location indicated by an address (column 2, lines 5 – 19; e.g., Figures 2A, and 2B). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further combine the recording of timestamp information in firmware as taught by the Benkeser/Hurvig combination with the addition routine taught by Matsuzaki, because the combination provides a mechanism to add elapsed timestamp information in the Benkeser invention via the indirect location register.

In regard to claim 10, incorporating the rejection of claim 8:

> *"reading the elapsed time value from an elapsed time register in a timestamp assist logic module, the elapsed time value corresponding to an elapsed time between a start of a segment execution and the step of reading the elapsed time; and*
> *"adding the elapsed time value to the contents stored in the location value register."*

Benkeser discloses a timer circuit used in computing holding time values (elapsed time; column 3, line 56). The timer circuit is used to compute the cumulative holding time, i.e., the accumulative time (adding the elapsed time) spent in execution of a segment (column 6, lines 17 – 44).

In regard to claim 11, incorporating the rejection of claim 8:

> *"reading the contents of a location value register, and*
> *"writing the contents read from the location value register to the first determined."*

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed and the accumulation of elapsed time, but neither Benkeser nor Hurvig explicitly discloses the reading or writing the contents of a location value. However, Matsuzaki discloses a hardware based operation wherein the steps of reading the contents of a memory designated by an address, writing the contents to a register having another value added to it, and then storing to

a location indicated by an address (column 2, lines 5 – 19; e.g., Figures 2A, and 2B). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further combine the recording of timestamp information in firmware as taught by the Benkeser/Hurvig combination with the addition routine taught by Matsuzaki, because the combination provides a mechanism to add elapsed timestamp information in the Benkeser invention via the indirect location register.

In regard to claim 12, incorporating the rejection of claim 8:

> *"generating a segment processing interrupt when a second segment is received for processing during one of the writing, reading, adding, and storing steps;*
> *"transmitting the segment processing interrupt to a processor;*
> *"interrupting segment processing; and*
> *"invoking a timestamp busy interrupt handler."*

Benkeser discloses that segment execution is interrupted by a time-slicing scheme to execute processes (column 6, lines 17 – 44). The step of generating and clearing an interrupt is inherent in a time-slice algorithm. Benkeser discloses that if a process is partially executed (elapsed time still in process, restarted with each time-slice), a cumulative holding time is computed (a time stamp) when the segment is fully executed after the time-slice interrupts.

In regard to claim 13, incorporating the rejection of claim 12:

> *"determining if the updating step is still in process;*
> *"determining if a timeout has been reached if the updating step is determined to still be in process;*
> *"restarting the updating step for the second segment; and*
> *"clearing the interrupt signal from the memory controller."*

Benkeser discloses that segment execution is interrupted by a time-slicing scheme to execute processes (column 6, lines 17 – 44). The step of generating and clearing an interrupt is inherent in a time-slice algorithm. Benkeser discloses that if a process is partially executed

(elapsed time still in process, restarted with each time-slice), a cumulative holding time is computed (a time stamp) when the segment is fully executed after the time-slice interrupts.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Benkeser et al., U.S. Patent 5,361,362 in view of Hurvig et al., U.S. Patent 6,507,592, as applied to claim 1 above, and further in view of Bhatt et al., U.S. Patent 4,636,967.

In regard to claim 5, incorporating the rejection of claim 1:

"disabling timestamp assist functions;

setting an elapsed time register to an initial value;

writing an initial address into a timestamp address register,

writing the initial address to an update address register; and

enabling the timestamp assist functions."

Benkeser discloses recording a timestamp corresponding to the beginning of a segment to be executed, and writes an initial address identifying the corresponding process into a field in the process table, but neither Benkeser nor Hurvig discloses disabling the timestamp function. However, Bhatt discloses enabling and disabling a time stamp function (column 3, lines 48 – 63) during initialization so that synchronization might be maintained. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Benkeser and Hurvig combination of recording of timestamp information in firmware with the timestamp enable/disable feature as taught by Bhatt, because the ability to enable/disable the timestamp provides a mechanism allowing proper synchronization of the recording as taught by Benkeser

with the underlying hardware during initialization or reset as taught by Bhatt at column 3, lines 48 – 62).

10. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benkeser et al., U.S. Patent 5,361,362, as applied to claim 14 above, in view of Matsuzaki et al., U.S. Patent 6,253,305.

In regard to claim 15, incorporating the rejection of claim 14:

"...wherein the timestamp assist logic module comprises:

an elapsed time module;"

See Benkeser column 5, line 47 – 48; Figure 1, ref 115.

"an update address register;"

See Benkeser column 5, line 38 – 40.

"a location value register."

A location value register is interpreted as having indirect addressing information. Benkeser discloses an elapsed time module and an update address register and a value field for elapsed time in the process table of Figure 3, but does not explicitly disclose location value register. However, Matsuzaki discloses a hardware based operation wherein the steps of reading the contents of a memory designated by an address, writing the contents to a register having another value added to it, and then storing to a location indicated by an address (column 2, lines 5 – 19; e.g., Figures 2A, and 2B). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the timestamp assist logic taught by Benkeser

with the location value register taught by Matsuzaki, because the combination provides a hardware value register to add elapsed timestamp information in the Benkeser invention via the indirect location register with greater execution time in hardware.

In regard to claim 16, incorporating the rejection of claim 15:

"...wherein the elapsed time module comprises an elapsed time register having an updated elapsed time value stored therein."

Benkeser discloses a cumulative hold time (an elapsed time value) stored in the process table of Figure 3.

Response to Arguments

11. Applicant's arguments filed on 6/25/2004 have been fully considered but they are not persuasive.

The Applicant has argued:

"Each of these claims contains elements directed to autonomous timestamp updates (without interaction from any central processing unit or complex processor system). Applicants respectfully submit, however, that Benkeser is directed to a method for adaptive job scheduling that requires processor interaction. Benkeser teaches that when a process is returned to a master process queue, the value of a counter register is included to reflect the holding time (Col. 5. lines 45 - 48). Benkeser teaches that a processor handles resetting of a hardware timer (Col. 5, Lines 42 - 45) and the processor is also the entity that uses the timer in returning the process to the process queue (Col. 6, Lines 32 -35). Thus, Benkeser does not teach that the updating of the timestamp is conducted

autonomously from any central processing unit or complex processor system, as claimed."

Examiner's response:

The claim 14 states: "a timestamp logic module configured to conduct timestamp update operations autonomously from the central processing unit by automatically updating a memory location specified by a value in the address register without interaction with the central processing unit." As written, the claim indicates that the timestamp module updates timestamp information autonomously apart from the CPU (column 5, lines 36 – 42). Therefore, the hardware timer circuit as disclosed in Benkeser still reads on the claims as presented because of the hardware timer circuit autonomously performs the updates, not the CPU. Also, there is no indication whatsoever of any firmware interaction in the updating process by the hardware timer circuit (column 5, lines 36 – 42).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence Shrader
Examiner
Art Unit 2124

24 September 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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